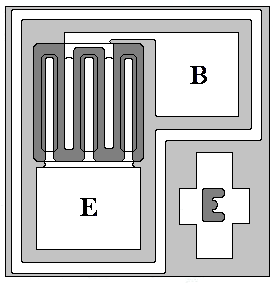
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.016”**



**.017”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” min**

**Backside Potential: Collector**

**Mask Ref: FEE**

**APPROVED BY: DK DIE SIZE .016” X .017” DATE: 5/16/22**

**MFG: SPRAGUE/ALLEGRO THICKNESS .008” P/N: 2N5089**

**DG 10.1.2**

#### Rev B, 7/19/02